IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the specification.

1. (Previously Presented) A memory cell comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the square feature size of the memory cell is not greater than $2F^2$.

2. (Previously Presented) The memory cell of claim 1, wherein the source comprises a buried layer.

3. (Previously Presented) The memory cell of claim 1, wherein the horizontal floating gate comprises a sub lithographic floating gate.

4. (Previously Presented) The memory cell of claim 1, wherein the horizontal floating gate comprises a sub lithographic floating gate defined by a spacer.

5. (Previously Presented) The memory cell of claim 1, wherein the horizontal floating gate comprises a self aligned floating gate.

6. (Currently Amended) A memory cell ~~having a square feature size of less than $4F^2$~~ comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel;

a substantially horizontal floating gate formed over at least a portion of the drain; and

a substantially vertical select gate formed substantially perpendicular to the horizontal floating gate in a trench, wherein the select gate is adjacent to the vertical channel, and the memory cell defines a square feature size of less than $4F^2$.

7. (Original) The memory cell of claim 6, wherein the memory cell has a minimum feature size corresponding to the horizontal floating gate and the vertical select gate.

8. (Original) The memory cell of claim 6 further comprising a select source and a select drain coupled to the select gate, wherein the select source, the select gate and the select drain form a select transistor.

9. (Previously Presented) The memory cell of claim 6, wherein the memory cell has a square feature size not greater than $2F^2$.

10. (Currently Amended) A memory cell ~~having a square feature size of less than $4.5F^2$~~ comprising:

a first transistor comprising a source, a drain and a gate, wherein the source and drain are arranged substantially vertically and the gate is formed substantially horizontally and positioned such that at least a portion of the gate overlies at least a portion of the drain; and

a select transistor coupled to the first transistor, comprising a source, a drain and a gate, wherein the gate of the select transistor is formed substantially vertically and perpendicular to the gate of the first transistor relative to a vertical plane, and the memory cell defines a square feature size of less than $4F^2$.

11. (Original) The memory cell of claim 10, wherein the drain of the first transistor has an upper surface and a lower surface and the source of the first transistor has an upper

surface and a lower surface and the upper surface of the source of the first transistor is located below the lower surface the drain of the first transistor.

12. (Original) The memory cell of claim 10, wherein the source and drain of the first transistor are shared as the source and drain of the select transistor.

13-14. (Canceled)

15. (Currently Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a horizontal first n-type layer formed over a substrate;

a p-type layer formed over the first n-type layer;

a horizontal second n-type layer formed over the p-type layer;

a horizontal floating gate formed over the substrate; and

a vertical select gate formed over the substrate, wherein the p-type layer forms a vertical channel, the first n-type layer forms a buried source and the second n-type layer forms a drain and the memory device has a square feature size of less than $4F^2$.

16. (Currently Amended) The memory device of claim 15, wherein the vertical select gate is formed substantially perpendicular to the horizontal floating gate and the floating gate is dimensioned so as to define a sublithographic floating gate.

17-19. (Canceled)

20. (Currently Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate;

a p-type layer formed over the first n-type layer;

a second n-type layer formed over the p-type layer;

a floating gate formed over the substrate;

a trench formed in the p-type layer; and

a select gate formed on a sidewall of the trench, wherein the memory device defines a square feature size of less than $4F^2$.

21. (Currently Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate forming a source;

a p-type layer formed over the first n-type layer forming a vertical channel;

a second n-type layer formed over the p-type layer forming a drain;

a tunnel oxide layer formed over at least a portion of the second n-type layer;

a first poly layer formed over at least a portion of the tunnel oxide layer;

trenches formed in the p-type layer; and

a select gate formed on sidewalls of the trenches, wherein the memory device defines a square feature size of less than $4F^2$.

22. (Currently Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a substrate having at least one semiconductor layer, said substrate comprising:~~comprising:~~

a buried source formed in the substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel;

a tunnel oxide layer formed over at least a portion of the drain;

a floating gate formed over the tunnel oxide layer such that at least a portion of the floating gate overlies at least a portion of the drain;

a select trench formed in the substrate;

a select gate formed along sidewalls of the select trench;

an active trench formed generally over the drain; and

a conductive layer formed in the active trench, wherein the memory device has a square feature size of less than $4F^2$.

23. (Currently Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench formed in the p-type layer;

a vertical select gate formed in the select trench;

digitlines formed over, and capable of electrical communication with the second n-type layer;

a floating gate formed over the p-type layer such that at least a portion of the floating gate overlies at least a portion of the second n-type layer; and

wordlines formed over the substrate and the digitlines, wherein the memory device has a square feature size of less than $4F^2$.

24. (Currently Amended) A memory device ~~having a square feature size of less than $4F^2$~~ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench formed in the substrate;

a vertical select gate formed in the select trench;

a conductive layer formed over at least a portion of the second n-type layer;

a first spacer formed on the conductive layer;

a tunnel oxide layer formed over at least a portion of the substrate;

a polysilicon layer formed on the tunnel oxide layer; and

an oxide layer formed on the polysilicon layer, wherein the memory device has a square feature size of less than $4F^2$.

25. (Previously Presented) The memory device of claim 24, wherein the conductive layer comprises a tungsten layer.

26. (Currently Amended) A memory device comprising:

a first n-type layer formed over a substrate defining a source;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer defining a drain;

a select trench formed in the p-type layer;

a select gate formed substantially vertically~~vertical~~ in the select trench; and

a floating gate formed horizontally over the p-type layer so as to avoid the select trench wherein the floating gate is dimensioned so as to define a sublithographic floating gate and the memory device has a square feature size of less than $4F^2$.

27. (Original) The memory device of claim 26, further comprising a tunnel oxide layer formed over the substrate.

28. (Original) The memory device of claim 27, further comprising digitlines and wordlines formed over the substrate.

29. (Original) The memory device of claim 28, wherein the wordlines are above the digitlines.

30. (Original) The memory device of claim 29, wherein the wordlines comprise a poly-WSi layer.

31. (Original) The memory device of claim 30, wherein the digitlines comprise at least one tungsten layer.

32. (Original) The memory device of claim 31, wherein the digitlines are above at least a portion of the drain.

33. (Original) The memory device of claim 32 further comprising a spacer formed between the digitlines and the wordlines.

34. (Currently Amended) The memory device of claim 26, wherein the drain ~~is~~ comprises a dopant implanted into an active area~~doped with Boron~~.

35. (Original) The memory device of claim 26, wherein the floating gate comprises tunnel oxide, polysilicon and oxide layers.

36. (Original) The memory device of claim 26, wherein the floating gate is self aligned.

37.-68. (Canceled)

69. (Currently Amended) A memory device comprising:

a substrate;

a buried source formed in the substrate;

a first layer formed over the substrate;

a first drain formed in the first layer generally over the buried source defining a first substantially vertical channel therebetween;

a trench formed in the first layer;

a select gate formed in the trench; and

a horizontal first floating gate formed over the first layer adjacent to the trench and proximate to the first substantially vertical channel, wherein the first floating gate is dimensioned so as to define a sublithographic gate and the square feature size of the memory cell is not greater than $2F^2$.

70. (Previously Presented) The memory device according to claim 69, further comprising:

a second drain formed in the first layer generally over the buried source defining a second substantially vertical channel therebetween; and

a second floating gate formed over the first layer adjacent to the trench and proximate to the second substantially vertical channel, wherein the

71. (Previously Presented) The memory device according to claim 69, wherein the floating gate defines a horizontal floating gate arranged over the first layer such that at least a portion of the floating gate overlies at least a portion of the drain.

72. (Previously Presented) The memory device according to claim 69, wherein the floating gate defines a horizontal floating gate further arranged generally above the substantially vertical channel.

73. (Previously Presented) The memory device according to claim 69, wherein the trench extends through the first layer to the buried source.

74. (Currently Amended) A memory device comprising:

a first layer defining a source;

a second layer formed over the first layer;

a drain formed in the second layer generally over the source defining a substantially vertical channel therebetween;

a trench formed in the second layer;

a select gate formed in the trench; and

a horizontal floating gate formed over the second layer adjacent to the trench so as to avoid extending vertically down into trench below the second layer~~.~~ , wherein the floating gate is dimensioned so as to define a sublithographic gate and the square feature size of the memory cell is not greater than $2F^2$.

75. (Previously Presented) The memory device according to claim 74, wherein the floating gate defines a horizontal floating gate arranged over the second layer such that at least a portion of the floating gate overlies at least a portion of the drain.

76. (Previously Presented) The memory device according to claim 74, wherein the trench extends through the second layer and into the first layer.

77. (Previously Presented) The memory device according to claim 74, wherein the floating gate defines a horizontal floating gate further arranged generally above the substantially vertical channel.

Please add the following new claims:

78. (New) The memory cell according to claim 10, wherein the memory cell is defined by a square feature size of $2F^2$.

79. (New) The memory device according to claim 15, wherein the memory cell is defined by a square feature size of $2F^2$.

80. (New) The memory device according to claim 20, wherein the memory cell is defined by a square feature size of $2F^2$.

81. (New) The memory device according to claim 21, wherein the memory cell is defined by a square feature size of $2F^2$.

82. (New) The memory device according to claim 22, wherein the memory cell is defined by a square feature size of $2F^2$.

83. (New) The memory device according to claim 23, wherein the memory cell is defined by a square feature size of $2F^2$.

84. (New) The memory device according to claim 24, wherein the memory cell is defined by a square feature size of $2F^2$.

85. (New) The memory device according to claim 26, wherein the memory cell is defined by a square feature size of $2F^2$.

86. (New) The memory cell according to claim 6, wherein the select gate is the only substantially vertical gate in the memory cell.

87. (New) The memory cell according to claim 10, wherein the gate of the first transistor is the only gate that is arranged substantially vertically in the memory cell.

88. (New) The memory device according to claim 21, wherein the select gate is the only gate that is arranged within the trenches.

89. (New) The memory device according to claim 22, wherein the select gate is the only gate that is arranged within the select trench.

90. (New) The memory device according to claim 23, wherein the select gate is the only vertical gate that is arranged within the select trench.

91. (New) The memory device according to claim 24, wherein the select gate is the only vertical gate that is arranged within the select trench.

92. (New) The memory device according to claim 26, wherein the select gate is the only vertical gate that is arranged within the select trench.